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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,911	MIN ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-16 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-11,14-16 and 35* is/are rejected.

7)☒ Claim(s) *7,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The previous indication of allowable subject matter has been withdrawn in view of the new grounds of rejection presented below. The finality of the previous Office Action has been withdrawn.

The after-final amendment filed March 24, 2006 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogura et al. (US Pat. 6,388,293, hereinafter Ogura).

Regarding claims 1-3, Figure 19 of Ogura discloses a control gate pattern (132L/242L) disposed over a semiconductor substrate 10 and comprising a tunnel insulation pattern 132a (silicon oxide), a trap insulation pattern (132b) (silicon nitride), a blocking insulation pattern 132c (silicon oxide) and a control gate 242L, which are stacked (col. 18, lines 5-15 and col. 20, lines 19-21); a selection gate electrode 241 disposed over the semiconductor substrate at one side and extending over substantially the entire top portion of the control gate pattern; a gate insulation pattern 401/402/103 interposed between the selection gate electrode and the semiconductor substrate, and between the selection gate electrode and the control gate pattern; a

cell channel region 212L/211/212R comprising a first channel region 212L defined in the semiconductor substrate under the control gate pattern and a second channel region 211R defined in the semiconductor substrate under the selection gate electrode; and drain/source regions (221/222) formed in the semiconductor substrate at respective sides of the cell channel region, the drain region 221 being in contact with the first channel region 212L and the source region being 222 in contact with the second channel region 212R.

Regarding claim 5, Figure 19 of Ogura discloses the thickness of the gate insulation pattern 401/402/103 (at region 103) is less than the sum of the thickness of the tunnel insulation pattern, the trap insulation pattern, and the blocking insulation pattern.

Claims 1-5 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Lung (US PGPub 2002/0145160).

Regarding claims 1-3, Figure 2 of Lung discloses a control gate pattern (206 and 205) disposed over a semiconductor substrate 201 and comprising a tunnel insulation pattern, a trap insulation pattern, a blocking insulation pattern, and a control gate electrode 206, which are stacked. Note that layer 205 is an ONO layer (paragraph [0023]). Therefore, the first oxide layer is the tunnel insulation pattern, the nitride layer is the trap insulation pattern, and the second oxide layer is the blocking insulation pattern. Figure 2 of Lung further discloses a selection gate electrode 207 disposed over the semiconductor substrate at one side and extending over substantially the entire top portion of the control gate pattern; a gate insulation pattern (208 and

part of 205) interposed between the selection gate and the semiconductor substrate, and between the selection gate and the control gate; a cell channel region comprising a first channel region defined in the semiconductor substrate under the control gate pattern and a second channel region defined in the substrate under the selection gate; and drain/source regions (203/202) formed in the substrate at respective sides of the cell channel region, the drain region 203 being in contact with the first channel region and the source region 202 being in contact with the second channel region. Note that the labels "control gate" and "select gate" are essentially a recitation of intended use that does not structurally distinguish the claimed invention over the prior art. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In this case, the electrode 206 is capable of operating as either a select gate or a control gate, depending on how the voltages are applied.

Regarding claims 4 and 35, Figure 2 of Lung discloses the selection gate electrode 207 covers one sidewall and the top surface of the control gate electrode 206 and is self-aligned to the other sidewall of the control gate electrode.

Regarding claim 5, Figure 2 of Lung discloses the thickness of the gate insulation pattern (portion 208) is less than the total thickness of the tunnel insulation pattern, the trap insulation pattern, and the blocking insulation pattern (all of which make up layer 205).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lung in view of Kawahara et al. (US Pat. 6,785,165, hereinafter Kawahara).

Regarding claims 8-10 and 14, Figure 2 of Lung discloses a first control gate pattern (206 and 205) disposed over a semiconductor substrate 201 and comprising a tunnel insulation pattern, a trap insulation pattern, a blocking insulation pattern, and a control gate electrode 206, which are stacked. Note that layer 205 is an ONO layer (paragraph [0023]). Therefore, the first oxide layer is the tunnel insulation pattern, the nitride layer is the trap insulation pattern, and the second oxide layer is the blocking insulation pattern. Figure 2 of Lung further discloses a first selection gate electrode 207 disposed over the semiconductor substrate at one side and extending over substantially the entire top portion of the control gate pattern; a first gate insulation pattern (208 and part of 205) interposed between the selection gate and the semiconductor substrate, and between the selection gate and the control gate; and a first cell channel region comprising a first channel region defined in the semiconductor substrate under the control gate pattern and a second channel region defined in the substrate under the selection gate. Note that the labels "control gate" and "select gate" are essentially a recitation of intended use that does not structurally distinguish the claimed invention over the prior art. A recitation of the intended use

of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In this case, the electrode 206 is capable of operating as either a select gate or a control gate, depending on how the voltages are applied. The difference between Lung and the claimed invention is a second control gate pattern, a second selection gate electrode, a second gate insulation pattern, and a second cell channel region, wherein the first and second selection gate electrodes are disposed symmetrically over the substrate. Figures 40-45 of Kawahara discloses first and second control gate patterns (MG1 and MG2) and first and second select gate electrodes (SG1 and SG2) disposed symmetrically on a substrate, wherein the control gate patterns are disposed between the selection gate electrodes. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Lung by including a second set of electrodes on the substrate disposed in the manner taught by Kawahara. The ordinary artisan would have been motivated to modify Lung in the manner described above for the purpose of increasing the capacity of the memory cell.

Regarding claim 11, Figure 2 of Lung discloses the first selection gate electrode 207 covers one sidewall and the top surface of the first control gate electrode 206 and is self-aligned to the other sidewall of the control gate electrode. Therefore, it would also be obvious to second set of electrodes arranged in this manner for the purpose of simplifying the production process.

Regarding claim 15, Figure 2 of Lung discloses a first source region 202 in contact with the second channel region of the first cell channel region and a drain region 203 in contact with the first channel region of the first cell channel region. It would have been further obvious to

have the first and second sets of electrodes arranged with a common drain region as taught by Kawahara (Figure 45) for the purpose of minimizing later space occupied by the memory cell. When arranged in this manner, a second source region will be in contact with the second channel region of the second cell channel region, and the common drain region will be in contact with the first channel region of the second cell channel region.

Regarding claim 16, Figure 2 of Lung discloses the thickness of the gate insulation pattern (portion 208) is less than the total thickness of the tunnel insulation pattern, the trap insulation pattern, and the blocking insulation pattern (all of which make up layer 205).

Allowable Subject Matter

The indicated allowability of claims 4 (rewritten as claim 35), 6 (incorporated into claim 1), and 8 is withdrawn in view of the newly discovered reference(s) to Lung and a new interpretation of Ogura.

Claims 7, 12, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application

or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

April 3, 2006

SPE Kenneth Parker
TC2800